5. SUMMARY OF THE INVENTION

A method of forming a gate oxide on a surface such as a transistor body region is shown where a metal layer is deposited by thermal evaporation on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table. The metal layer is then oxidized to convert the metal layer to a gate oxide. In one embodiment, the metal layer includes yttrium (Y). In one embodiment, the metal layer includes gadolinium (Gd). One embodiment of the invention uses an electron beam source to evaporate the metal layer onto the body region of the transistor. The oxidation process in one embodiment utilizes a krypton(Kr)/oxygen (O_2) mixed plasma process.

In addition to the novel process of forming a gate oxide layer, a transistor formed by the novel process exhibits novel features that may only be formed by the novel process. Thermal evaporation deposition of a metal layer onto a body region of a transistor preserves an original smooth surface roughness of the body region in contrast to other prior deposition methods that increase surface roughness. The resulting transistor fabricated with the process of this invention will exhibit a gate oxide/body region interface with a surface roughness variation as low as 0.6 nm.

6. ISSUES PRESENTED FOR REVIEW

Whether claims 1-7, 14-20, 22-28, 54-56, and 58-60 were properly rejected under 35 U.S.C.§103(a) as being unpatentable over Maiti et al. (U.S. 6,020,024) in view of Dalal et al. (U.S. 4,797,593).

7. GROUPING OF CLAIMS

The claims 1-7, 14-20, 22-28, 54-56, and 58-60 are grouped together. The claims stand or fall together.

8. ARGUMENT

Claims 1-7, 14-20, 22-28, 54-56, and 58-60 were rejected under 35 USC § 103(a) as being unpatentable over Maiti et al. (U.S. 6,020,024) in view of Dalal et al. (U.S. 4,797,593).

The rejection states that, "In addition to the deposition of metal oxide gate dielectric layer using CVD, it is possible to deposit a metal layer by sputtering and subsequently perform an oxidation step on the deposited layer and also perform CVD of a metallic oxide to form a composite metal layer." The rejection further states, "Dalal discloses the formation of a tantalum layer formed by an evaporation process."

Maiti appears to show a CVD or alternatively a sputtering deposition method used to deposit a metal layer used to form a gate oxide. However, Maiti does not show, teach or suggest **evaporation depositing** a metal layer on the body region. Maiti does not appear to recognize the advantages of using an evaporation depositing technique as discussed in Applicant's specification. For example, on page 7, lines 10-29, the specification discusses processing advantages such as the high purity of available starting materials in evaporation depositing; amorphous deposition; a smooth interface in combination with a thin deposited layer; and low substrate processing temperature. Applicant's specification teaches away from techniques such as sputtering on page 3, lines 12-21, while Maiti appears to equate sputtering with CVD. In contrast, Applicant's independent claims each include evaporation depositing a metal layer on the body region.

Dalal appears to show evaporation depositing or alternatively RF sputtering a layer of tantalum metal 28 to form a diode contact as shown in Figure 1E. However, nothing in the Dalal reference mentions formation of **gate oxides** in **transistors** as included in Applicant's claims. Because the Dalal reference does not show gate oxide structures, Applicant respectfully submits that there is no motivation to combine the references. As taught by the Applicant in the specification, gate oxide structures present specific technical problems including surface roughness and elemental purity issues. Applicant respectfully submits, the mere fact that Dalal discusses evaporation depositing does not teach how to achieve advantages taught by Applicant. Similar to Maiti, as discussed above, Dalal appears to equate evaporation depositing with sputtering (col. 4, lines 56-58), which is contrary to the teachings of Applicant's specification.

The Office Action mailed on May 7, 2003 further stated:

> The use of Dalal in the rejection is used to show the advantages of depositing a metal layer by E-beam evaporation on to a substrate it is also used to show that one of ordinary skill in the art would view this method to be analogous to sputtering. Maiti is used to show the IIB (sic) rare earth metals have been used

in the formation of gate oxides. With knowledge in the art it would be obvious that the bridge used in this case would be the fact that Dalal equates evaporation with sputtering.

Contrary to the statements above, Dalal does not appear to suggest any advantages of evaporation depositing over sputtering. In fact, as noted by the Examiner, and found in col. 4, lines 56-58, Dalal appears to equate evaporation depositing with sputtering. Applicant respectfully submits Dalal does not teach any reason to select evaporation depositing over sputtering. Further, as argued above, Applicant respectfully submits Dalal does not teach any advantages or reasons to choose evaporation depositing over sputtering in the context of gate oxides in transistors.

Any motivation to combine Dalal as suggested in the Office Action mailed on May 7, 2003 appears to come from impermissible hindsight having the benefit of Applicant's disclosure. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01.

Because there is no motivation to combine the Dalal reference with the Maiti reference, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 1, 14, 22, 54, 58. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

9. SUMMARY

It is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C. §103 has not been established. Therefore, it is respectfully requested that the rejections of claims 1-29, 54-60, and 67-69 be reconsidered and withdrawn so that the claims will be in condition for

allowance. The Examiner is invited to telephone Applicant's attorney, David Peterson, at (612) 373-6944 to facilitate prosecution of this application. Should the Board be of the opinion that any rejected claim is allowable in amended form, an explicit statement to that effect is also respectfully requested. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KIE Y. AHN ET AL.

By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 7th day of July, 2003

Amy Moriarty _____

Name Signature

APPENDIX I

The Claims on Appeal

1. (Original) A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table; and

oxidizing the metal layer to form a metal oxide layer on the body region.

2. (Original) The method of claim 1, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

3. (Original) The method of claim 1, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

4. (Original) The method of claim 3, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

5. (Original) The method of claim 1, wherein evaporation depositing the metal layer includes evaporation depositing at a substrate temperature of approximately 150 - 400 °C.

6. (Original) The method of claim 1, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

7. (Original) The method of claim 1, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

8. (Original) The method of claim 1, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O2) mixed plasma process.

9. (Original) A method of forming a gate oxide on a transistor body region, comprising:

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table; and

oxidizing the metal layer using a krypton(Kr)/oxygen (O2) mixed plasma process to form a metal oxide layer on the body region.

10. (Original) The method of claim 9, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

11. (Original) The method of claim 9, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

12. (Original) The method of claim 11, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

13. (Original) The method of claim 9, wherein evaporation depositing the metal layer includes evaporation depositing at a substrate temperature of approximately 150 - 400 °C.

14. (Original) A method of forming a transistor, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region; and

coupling a gate to the metal oxide layer.

15. (Original) The method of claim 14, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

16. (Original) The method of claim 14, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

17. (Original) The method of claim 16, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

18. (Original) The method of claim 14, wherein evaporation depositing the metal layer includes evaporation depositing at a substrate temperature of approximately 150 - 400 °C.

19. (Original) The method of claim 14, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

20. (Original) The method of claim 14, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

21. (Original) The method of claim 14, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O2) mixed plasma process.

22. (Original) A method of forming a memory array, comprising:

forming a number of access transistors, including:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

23. (Original) The method of claim 22, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

24. (Original) The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

25. (Original) The method of claim 24, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

26. (Original) The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing at a substrate temperature of approximately 150 - 400 °C.

27. (Original) The method of claim 22, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

28. (Original) The method of claim 22, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

29. (Original) The method of claim 22, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O2) mixed plasma process.

30. - 53. (Previously Withdrawn)

54. (Original) A transistor formed by the process, comprising:

forming a body region coupled between a first source/drain region and a second source/drain region;

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region; and

coupling a gate to the metal oxide layer.

55. (Original) The transistor of claim 54, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

56. (Original) The transistor of claim 54, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

57. (Original) The method of claim 54, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O2) mixed plasma process.

58. (Original) A method of forming an information handling system, comprising:

forming a processor;

forming a memory array, including:

forming a number of access transistors, including:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

forming a system bus that couples the processor to the memory array.

59. (Original) The method of claim 58, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

60. The method of claim 58, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.

61. - 66. (Previously Withdrawn)

67. (Previously Added) A method of forming a transistor, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region, the metal being chosen from a group consisting of the group IIIB elements and the rare earth series of the periodic table;

oxidizing the metal layer using a krypton(Kr)/oxygen (O2) mixed plasma process to form a metal oxide layer on the body region; and

coupling a gate to the metal oxide layer.

68. (Previously Added) The method of claim 67, wherein evaporation depositing the metal layer includes depositing a metal layer, the metal layer being chosen from a group consisting of yttrium and gadolinium.

69. (Previously Added) The method of claim 67, wherein evaporation depositing the metal layer includes evaporation depositing by electron beam evaporation.